HIGH-SPEED SIGNAL LEVEL DETECTOR

Background of the Invention

1. Field of the Invention

This invention relates generally to high-speed signal level detectors, and more particularly to a high-speed signal level detector that employs the high gain and high bandwidth of an inverter to perform a comparison.

2. Description of the Prior Art

The high-speed level detector for the input signal is very important for ensuring a fast response to incoming data for a high-speed data recovery circuit. Traditionally, a high-speed data recovery circuit employs an averaging technique to detect the input signal level, or employs an op-amp type comparator. Both techniques require significant power to achieve the requisite bandwidth and speed requirements. Further, the circuit is thus limited to the circuit bandwidth to detect the signal strength.

In view of the foregoing, it would be both beneficial and advantageous to provide a high-speed level detector capable of achieving the desired high-speed level detection without demanding the substantial power consumption required when using either the averaging technique or a high-bandwidth op-amp type comparator.

Summary of the Invention

To meet the above and other objectives, the present invention provides a high-speed signal level detector that employs the high gain and high bandwidth of an inverter to perform a comparison. The high-speed signal level detector is capable of achieving the desired high-speed level detection without demanding the substantial power consumption required when using either the averaging technique or a high bandwidth op-amp type comparator. This high-speed signal level detector advantageously 1) functions independently of the circuit bandwidth to achieve the desired fast response, 2) is very simple to implement, and 3) requires less area to implement than circuits that employ more traditional design techniques such as using averaging or high bandwidth op-amp type comparison architectures.

According to one embodiment, a signal level detector comprises:

a first DC error amplifier operational to generate a control signal in response to a reference signal and a feedback signal; and

a first inverter operational to generate the feedback signal in response to the first DC error amplifier control signal, wherein the first DC error amplifier control signal operates to set a switching point for the first inverter.

According to another embodiment, a signal level detector comprises:

first means for generating a first control signal in response to a first reference signal and further in response to a first feedback signal; and

second means for controlling the first feedback signal in response to the first control signal, wherein the first control signal operates to set a switching point for the second means.

According to yet another embodiment, a method of controlling a level detector comprises the steps of:

providing a DC error amplifier having a positive input, a negative input and operational to generate an output control signal;

driving the negative input via a desired reference voltage; and

driving the positive input via a self-biasing inverter feedback signal in response to the DC error amplifier output control signal to control a switching point associated with the self-biasing inverter.

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Brief Description of the Drawings

Other aspects and features of the present invention and many of the attendant advantages of the present invention will be readily appreciated, as the invention becomes better understood by reference to the following detailed description when considered in connection with the accompanying drawing figures thereof and wherein:

Figure 1 is a schematic diagram illustrating a high-speed signal level detector according to one embodiment of the present invention;

Figure 2 is a schematic diagram illustrating the controlled trigger point generator portion of the high-speed signal level detector circuit 10 depicted in Figure 1;

Figures 3A-3C show a schematic diagram illustrating a high-speed differential comparator that employs the high-speed signal level detector 10 shown in Figure 1 according to one embodiment of the present invention; and

Figure 4 is a graph depicting simulated plots of performance for the high-speed differential comparator shown in Figure 3.

While the above-identified drawing figures set forth particular embodiments, other embodiments of the present invention are also contemplated, as noted in the discussion. In all cases, this disclosure presents illustrated embodiments of the present invention by way of representation and not limitation. Numerous other modifications and embodiments can be devised by those skilled in the art which fall within the scope and spirit of the principles of this invention.

Detailed Description of the Preferred Embodiments

Figure 1 is a schematic diagram illustrating a high-speed signal level detector 10 according to one embodiment of the present invention. A high speed level detector for the input signal is very important for a high speed data recovery circuit to have a fast response to incoming data, as stated herein before. The working principle for the high-speed signal level detector 10 is by way of controlling the switching point of an inverter 12 that is comprised of transistors MP1, MN3 and MN4 to make a comparison. An error amplifier 13 can be seen to have its negative terminal connected to VTHR 14 that is generated via a reference source, and its positive terminal connected to the gates of inverter transistors MP1 and MN3. Due to the high DC gain of the error amplifier 13, its plus terminal will also be at VTHR, which will set the bias point of the inverter 12 in its high gain region. The control voltage (VCTL) 16 is the output of the error amplifier 13 that helps to adjust transistor MN4 (enumerated as number 18 within the oval containing transistors MN3 and MN4) to the requisite biasing point of the inverter 12.

Figure 2 is a schematic diagram illustrating the controlled trigger point generator portion 20 of the high-speed signal level detector circuit 10 depicted in Figure 1. The self-bias inverter 22 discussed herein before, is depicted within the oval containing transistors MN3 and MN4; while the amplifier 13, as stated herein before, operates as an error amplifier.

Looking now at Figures 3A-3C, a schematic diagram illustrates a high-speed differential comparator 30 that employs the high-speed signal level detector 10 shown in Figure 1 according to one embodiment of the present invention. An input reference voltage through a reference amplifier 32 and a resistor string 34 functions to generate the differential voltage for the high speed comparators 36, 38, one with VTHP 40 and another with VTHN 42. If the input signal is larger than (VTHP – VTHN), the output 44 through the logic will be changed high as shown in Figure 4. Since the amplitude for the application is AC, the high-speed differential comparator 30 employs AC coupling capacitors 46, 48 to eliminate the DC components of the signal.

Figure 4 is a graph depicting simulated plots of performance for the high-speed differential amplitude detector 30 shown in Figure 3. If the input signal is larger than (VTHP –VTHN), the output 44 through the logic will transition high, as stated herein before. Output transition plots are depicted for a plurality of different process corners, temperatures and voltages.

In view of the above, it can be seen the present invention presents a significant advancement in the art of high-speed level detector technology. Further, this invention has been described in considerable detail in order to provide those skilled in the amplitude level detector circuit art with the information needed to apply the novel principles and to construct and use such specialized components as are required. In view of the foregoing descriptions, it should further be apparent that the present invention represents a significant departure from the prior art in construction and operation. However, while particular embodiments of the present invention have been described herein in detail, it is to be understood that various alterations, modifications and substitutions can be made therein without departing in any way from the spirit and scope of the present invention, as defined in the claims which follow.